AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

Claims 1-33 (canceled).

34. (original) A DRAM process, comprising:

forming a deep trench capacitor in a semiconductor substrate;

defining an active area over the substrate to form a semiconductor pillar beside the deep trench capacitor and to form an isolation area;

forming a buried strap coupling with the deep trench capacitor in the substrate;

forming a gate dielectric layer on the pillar;

forming a word line including a multi-gate over the substrate, wherein the multi-gate is at least on three sidewalls of the pillar and is separated from the pillar by the gate dielectric layer;

forming a source/drain region in a top portion of the pillar; and

forming a bit line electrically connecting with the source/drain region,

wherein the pillar, the buried strap, the gate dielectric layer, the multi-gate and the source/drain region together constitute a transistor.

35. (original) The DRAM process of claim 34, wherein the buried strap is formed through out-diffusion of dopants from a contact portion of an inner electrode of the deep trench capacitor.

36. (original) The DRAM process of claim 34, wherein a mask layer for defining the active area overlaps with the deep trench capacitor.

37. (original) The DRAM process of claim 34, wherein the multi-gate is formed as a treble gate on three sidewalls of the pillar.

38. (original) The DRAM process of claim 37, wherein forming the gate dielectric layer and the word line including the treble gate comprises:

filling the isolation area with an insulating material;

recessing the insulating material to expose a first, a second, and a third sidewalls of the pillar above a predetermined level, wherein the first sidewall faces the deep trench capacitor and the second and third sidewalls are adjacent to the first sidewall;

forming a gate dielectric layer on the pillar;

forming a conductive layer over the substrate; and

patterning the conductive layer to form a word line including a treble gate, wherein the treble gate is formed on the first to third sidewalls and the top of the pillar.

39. (original) The DRAM process of claim 38, wherein the step of forming the source/ drain region in the top portion of the pillar comprises:

performing an ion implantation process using the word line as a mask.

40. (original) The DRAM process of claim 38, wherein the conductive layer comprises a doped polysilicon layer and a metal comprising layer on the doped polysilicon layer.

41. (original) The DRAM process of claim 38, further comprising:

forming a capping layer on the conductive layer before the conductive layer is

patterned, while the capping layer and the conductive layer are patterned successively to form a stacked word line structure; and

forming a spacer on sidewalls of the stacked word line structure.

42. (original) The DRAM process of claim 41, further comprising a step of forming a self-aligned contact (SAC) on the source/drain region before the bit line is formed for electrically connecting the source/drain region and the bit line.

43. (original) The DRAM process of claim 37, wherein forming the gate dielectric layer and the word line including the treble gate comprises:

filling the isolation area with an insulating material;

patterning the insulating material to form a trench in which the word line will be formed, the trench exposing a first sidewall of the pillar above a predetermined level and a portion of a second sidewall and a portion of a third sidewall of the pillar above the predetermined level, wherein the first sidewall faces the deep trench capacitor and the second and third sidewalls are adjacent to the first sidewall;

forming a gate dielectric layer on the pillar; and

forming the word line in the trench.

44. (original) The DRAM process of claim 43, wherein a top surface of the word line is lower than a top surface of the pillar.

45. (original) The DRAM process of claim 44, wherein the step of forming the bit line comprises:

forming an insulating layer in the trench covering the word line; and

forming a patterned conductive layer as a bit line directly contacting with the

source/drain region.

46. (original) The DRAM process of claim 34, wherein the multi-gate is formed as a surrounding gate that surrounds sidewalls of the pillar.

47. (original) The DRAM process of claim 46, wherein the width of the pillar is smaller than a feature size.

48. (original) The DRAM process of claim 47, wherein the width of the pillar is sufficiently small for inducing full depletion therein in use of the DRAM cell.

49. (original) The DRAM process of claim 46, wherein forming the gate dielectric layer and the word line including the surrounding gate comprises:

filling the isolation area with an insulating material;

patterning the insulating material to form a trench in which the word line will be formed, the trench exposing all sidewalls of the pillar above a predetermined level;

forming a gate dielectric layer on the pillar; and

forming the word line in the trench.

50. (original) The DRAM process of claim 49, wherein a top surface of the word line is lower than a top surface of the pillar.

51. (original) The DRAM process of claim 50, wherein the step of forming the bit line comprises:

forming an insulating layer in the trench covering the word line; and

forming a patterned conductive layer as a bit line directly contacting with the source/drain region.